

International  
**IR** Rectifier

AUTOMOTIVE MOSFET

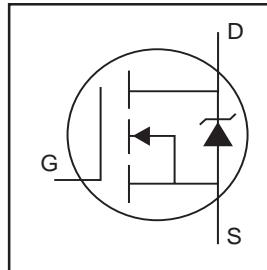
PD - 11371

**IRF1404Z**

HEXFET® Power MOSFET

**Features**

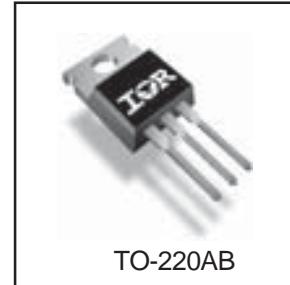
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$



$V_{DSS} = 40V$   
 $R_{DS(on)} = 3.7m\Omega$   
 $I_D = 75A$

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



TO-220AB

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	190	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	130	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	75	
$I_{DM}$	Pulsed Drain Current ①	750	
$P_D @ T_C = 25^\circ C$	Power Dissipation	220	W
	Linear Derating Factor	1.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	320	mJ
$E_{AS}$ (Tested )	Single Pulse Avalanche Energy Tested Value ⑥	480	
$I_{AR}$	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1N·m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{0JC}$	Junction-to-Case	—	0.67	°C/W
$R_{0CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{0JA}$	Junction-to-Ambient	—	62	

# IRF1404Z

Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

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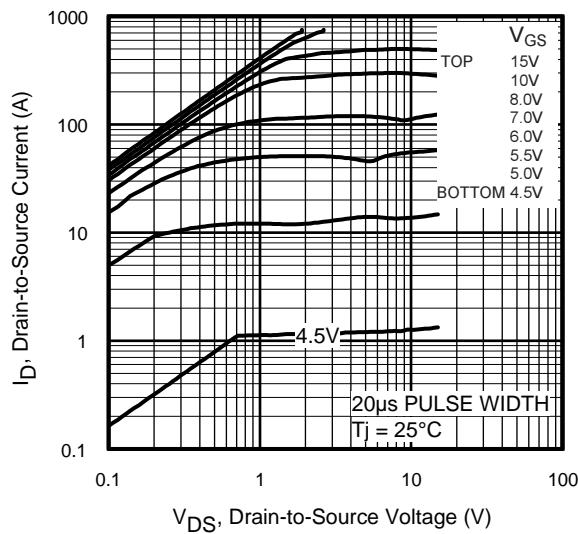
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.033	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	2.7	3.7	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$ , $I_D = 75\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\mu\text{A}$
$g_{\text{fs}}$	Forward Transconductance	170	—	—	V	$V_{\text{DS}} = 25\text{V}$ , $I_D = 75\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{\text{DS}} = 40\text{V}$ , $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 40\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -20\text{V}$
$Q_g$	Total Gate Charge	—	100	150	nC	$I_D = 75\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	—	31	—		$V_{\text{DS}} = 32\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller" Charge	—	42	—		$V_{\text{GS}} = 10\text{V}$ ③
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	18	—	ns	$V_{\text{DD}} = 20\text{V}$
$t_r$	Rise Time	—	110	—		$I_D = 75\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	36	—		$R_G = 3.0\ \Omega$
$t_f$	Fall Time	—	58	—		$V_{\text{GS}} = 10\text{V}$ ③
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{\text{iss}}$	Input Capacitance	—	4340	—	pF	$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	1030	—		$V_{\text{DS}} = 25\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	550	—		$f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	3300	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 1.0\text{V}$ , $f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	920	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 32\text{V}$ , $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	1350	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 0\text{V}$ to $32\text{V}$ ④

## Source-Drain Ratings and Characteristics

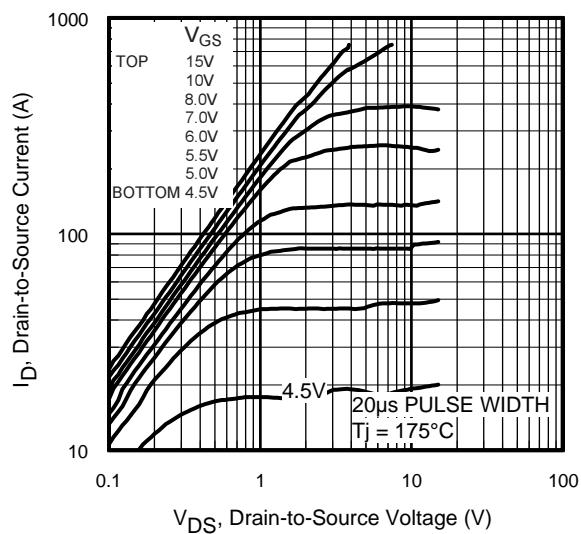
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
	Pulsed Source Current (Body Diode) ①	—	—	750		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$ , $I_S = 75\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ③
$t_{\text{rr}}$	Reverse Recovery Time	—	28	42	ns	$T_J = 25^\circ\text{C}$ , $I_F = 75\text{A}$ , $V_{\text{DD}} = 25\text{V}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	34	51	nC	$\text{di}/\text{dt} = 100\text{A}/\mu\text{s}$ ③
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

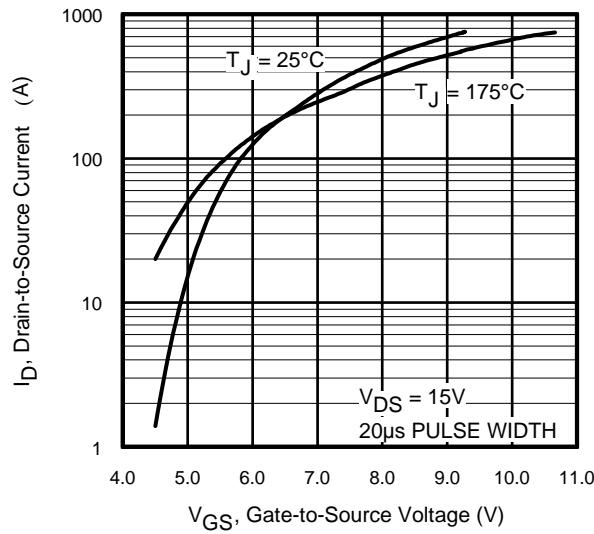
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{\text{Jmax}}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.11\text{mH}$  ⑤  $R_G = 25\Omega$ ,  $I_{\text{AS}} = 75\text{A}$ ,  $V_{\text{GS}} = 10\text{V}$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{\text{oss eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}$ .
- ⑤ Limited by  $T_{\text{Jmax}}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.



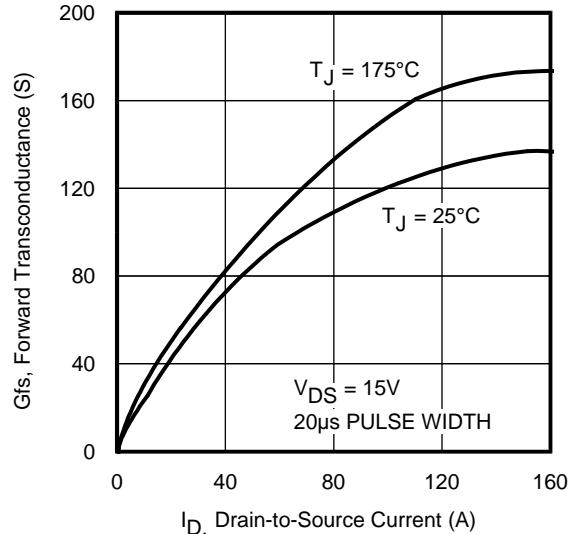
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



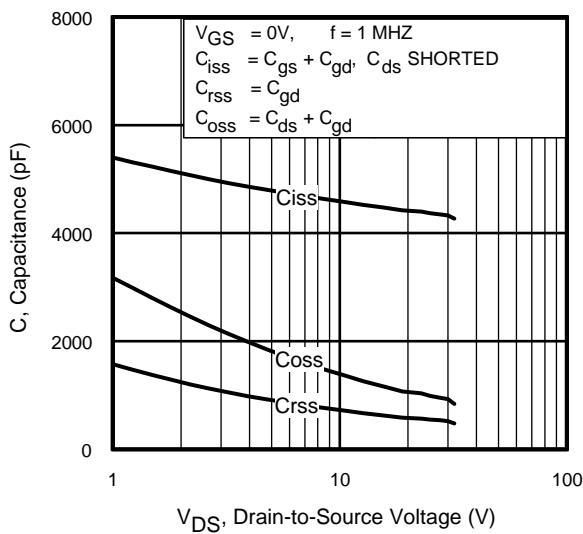
**Fig 3.** Typical Transfer Characteristics



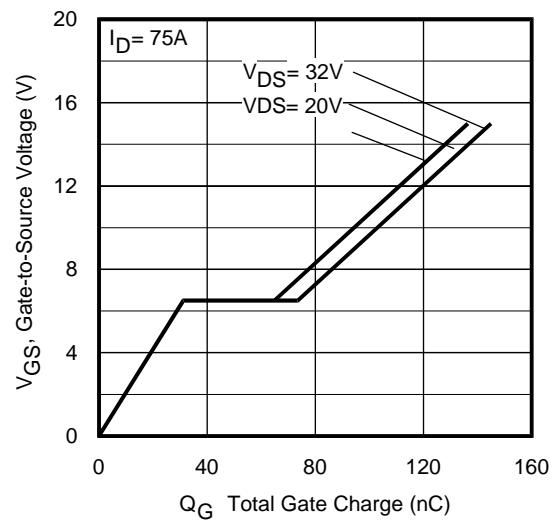
**Fig 4.** Typical Forward Transconductance Vs. Drain Current

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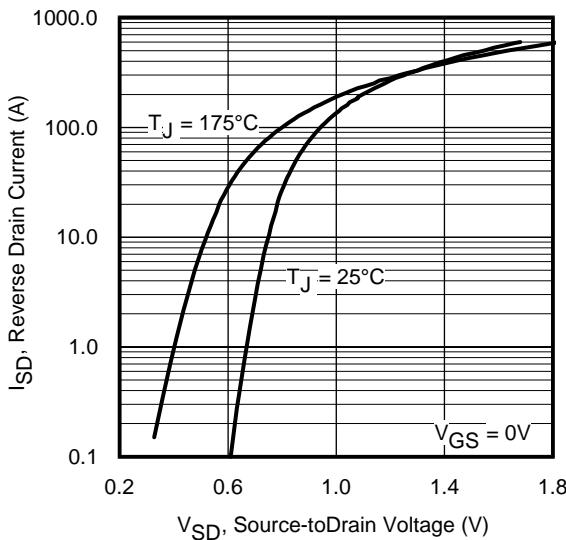
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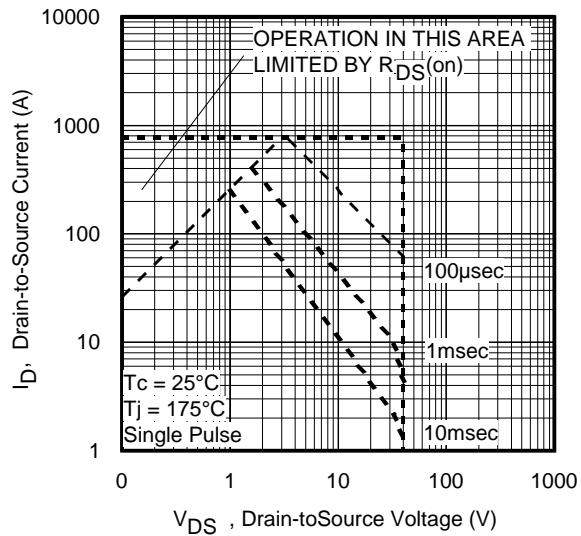
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



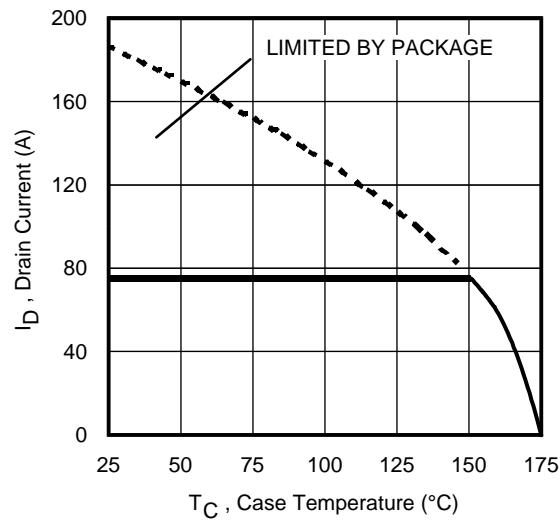
**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage



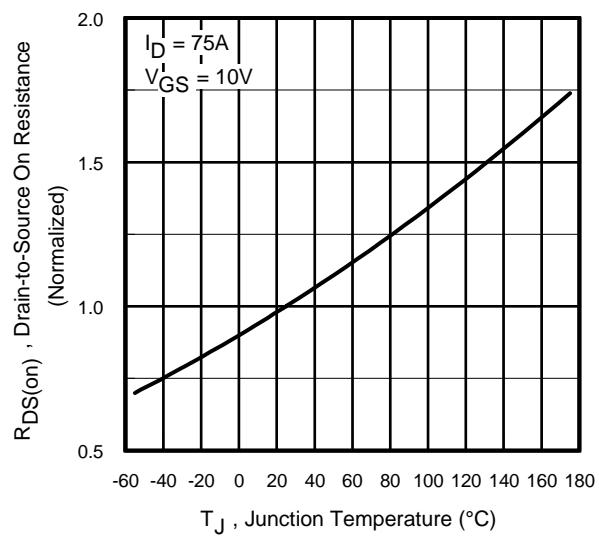
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



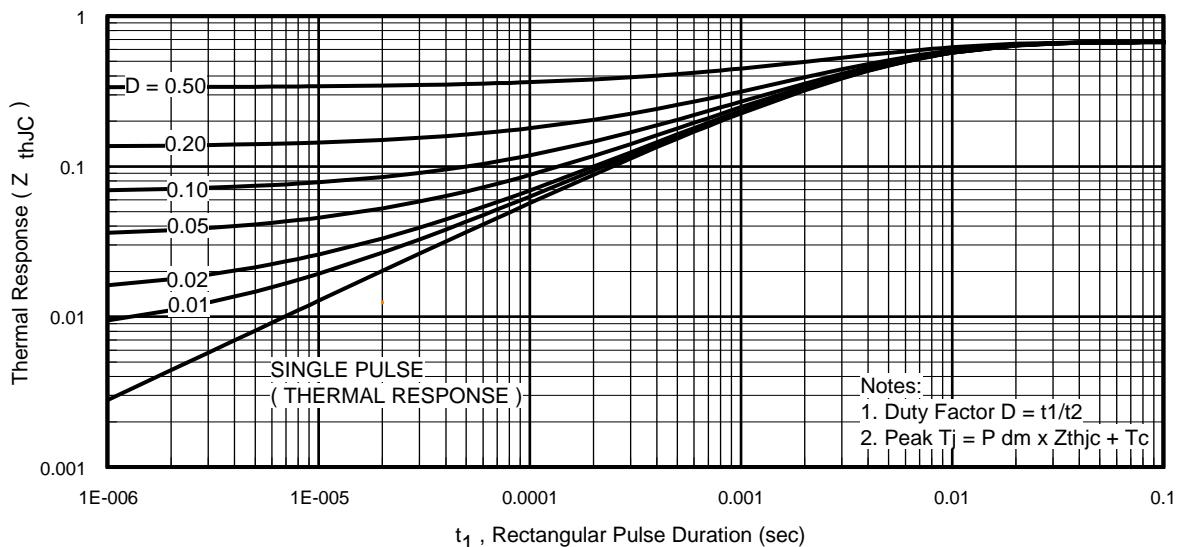
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs.  
Case Temperature



**Fig 10.** Normalized On-Resistance  
Vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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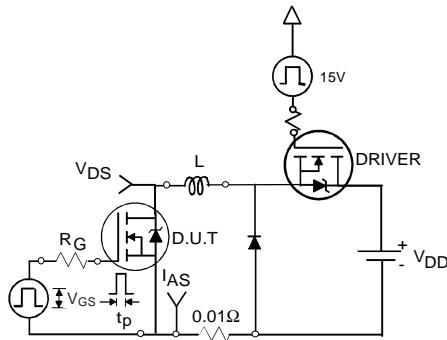


Fig 12a. Unclamped Inductive Test Circuit

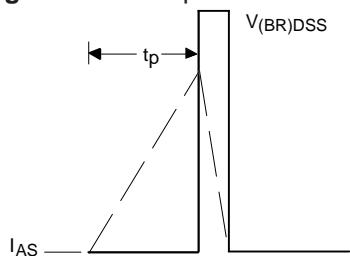


Fig 12b. Unclamped Inductive Waveforms

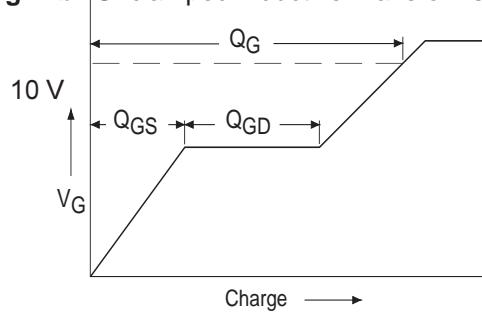


Fig 13a. Basic Gate Charge Waveform

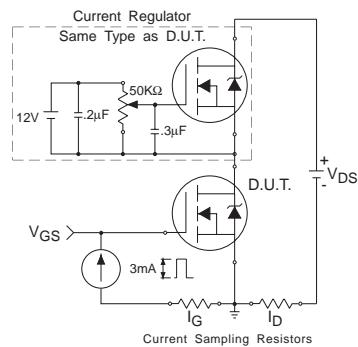


Fig 13b. Gate Charge Test Circuit

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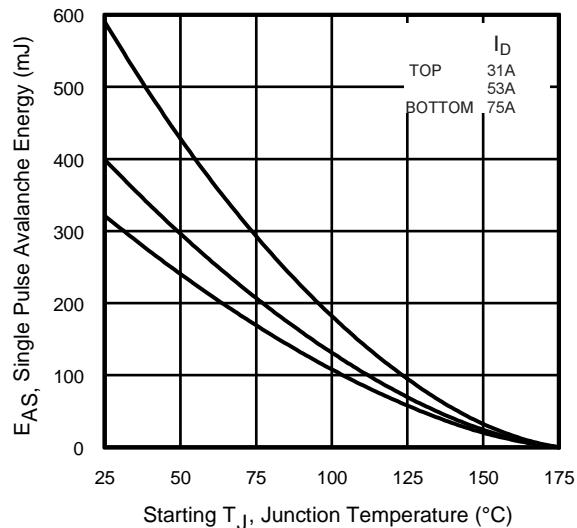


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

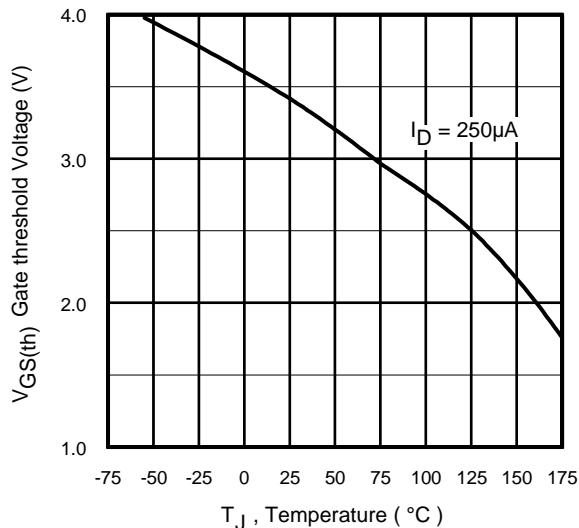


Fig 14. Threshold Voltage Vs. Temperature  
[www.irf.com](http://www.irf.com)

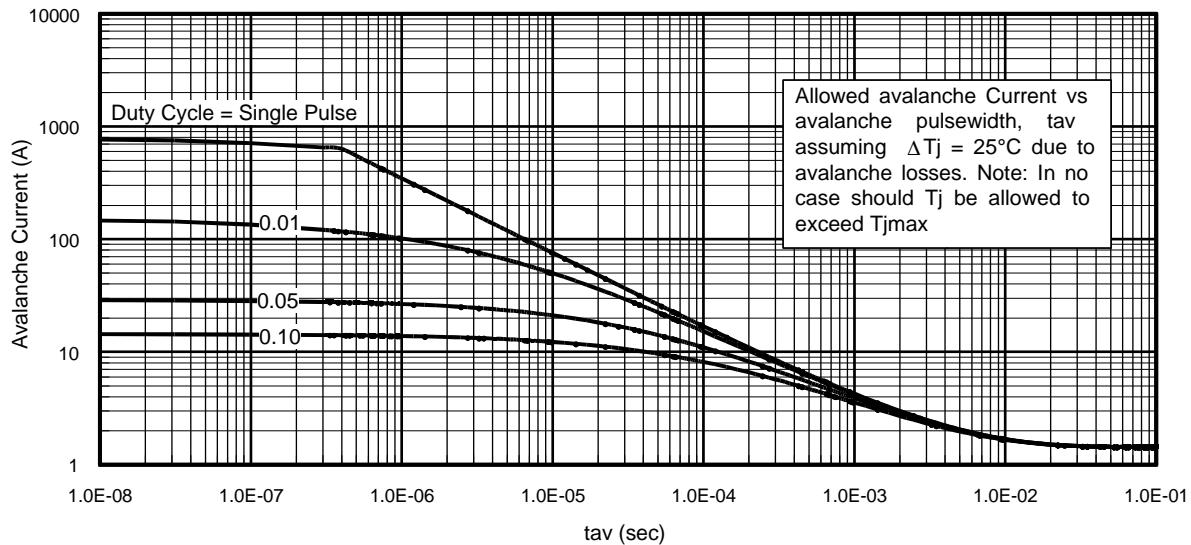


Fig 15. Typical Avalanche Current Vs.Pulsewidth

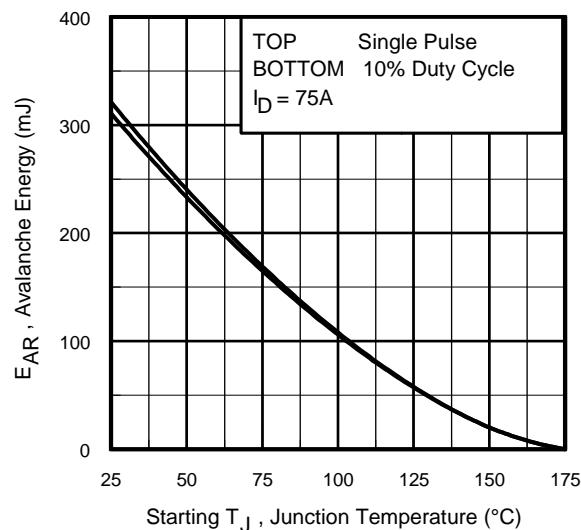


Fig 16. Maximum Avalanche Energy Vs. Temperature

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Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

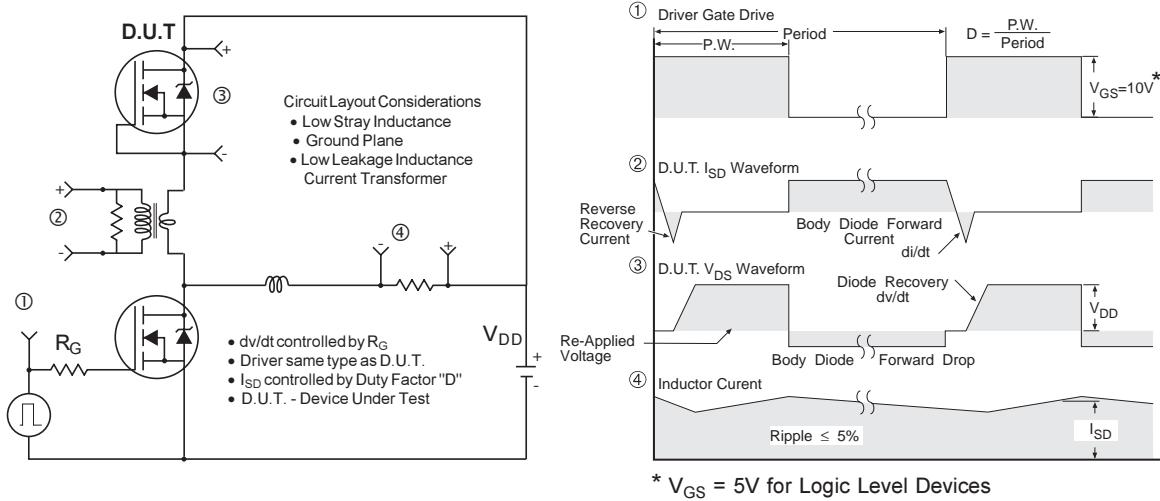
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ\text{C}$  in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.

D = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

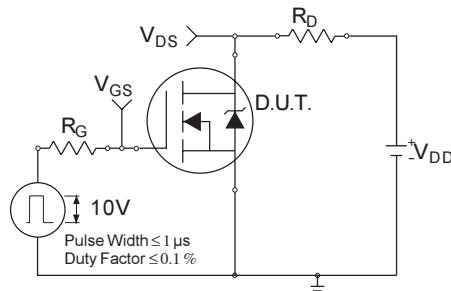
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

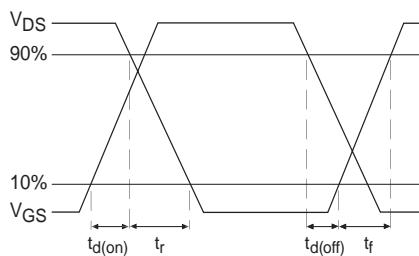
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



**Fig 18a.** Switching Time Test Circuit



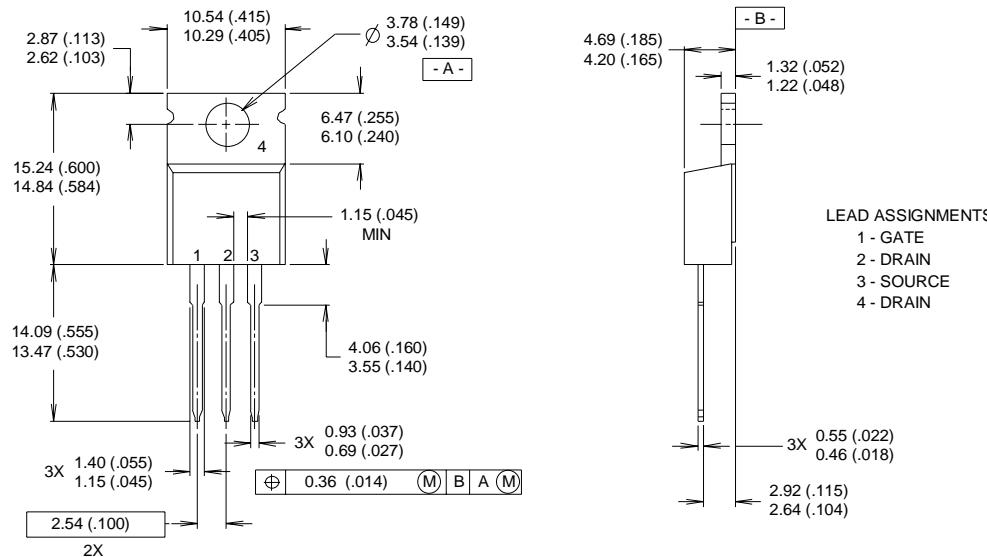
**Fig 18b.** Switching Time Waveforms

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## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



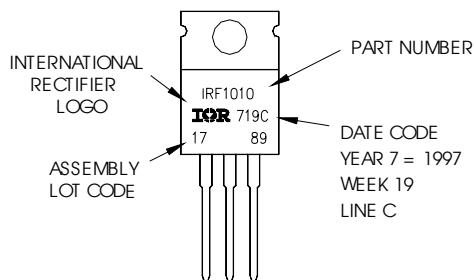
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.  
2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.  
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Automotive [Q101] market.  
Qualification Standards can be found on IR's Web site.

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**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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